UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/087,590	02/27/2002	Jered Donald Aasheim	MS1-1067US	3893

22801 7590 07/20/2004

LEE & HAYES PLLC
421 W RIVERSIDE AVENUE SUITE 500
SPOKANE, WA 99201

EXAMINER	
PEIKARI, BEHZAD	
ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 07/20/2004

12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/087,590	AASHEIM ET AL.	
	Examiner	Art Unit	
	B. James Peikari	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,15-20,22-26 and 28-44* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,15-20,22-26 and 28-44* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 May 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 9.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The substitute drawings filed on May 21, 2004 have been approved for entry by the examiner. Should the application be allowed, the drawings will be forwarded to the draftsperson for final review.

Claim Objections

2. The additional fees for claim 7, previously examined but now cancelled, have not been received.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-6, 15-20, 22-26 and 28-44 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Bruce et al., U.S. 6,000,006.

As presently written, the claims are quite broad, to the extent that they would have been taught by a system that utilized a random access memory to store logical-to-physical address mapping information for an associated flash memory, with all of the usual procedures utilized with such a map, such as reestablishing the map when a modification or erasure has occurred. Bruce et al. taught such a system. Note Figures 4 and 6 and column 6.

(a) As for a "list" of addresses from which a free one may be selected, note the "unified re-map table".

(b) As for the addresses representing "sectors", since flash memories are not radial disks, the term "sectors" is merely a convention to describe a given amount of data. Bruce et al., U.S. 6,000,006 even explains this in the Summary of the Invention "A 64 Mbit flash chip typically has 512-byte pages which happens to match the sector size for IDE and SCSI hard disks". Thus, "sectors" as used in the present invention is well within the scope of the Bruce et al. "pages".

(c) As for the selection of an address being "based on the ability of the physical sector to store the data without first being erased", selection of a free space instead of a full space clearly anticipates selecting "based on the ability of the physical sector to store the data without first being erased". The preference of a free space is fundamental to wear-leveling systems which direct write requests to unused or less-frequently-used memory areas. Bruce et al. explicitly teaches the use of wear-leveling, note column 4, lines 55 et seq.

(d) As for the claimed "forming" and "storing", this is simply entering the logical/physical address relationship into the table, as clearly taught throughout the reference.

(e) As for recreating the "data structure" after it has been erased, this simply means re-entering the logical/physical address relationship into the table, which must be done by Bruce et al. every time a relationship changes.

5. Claims 1-6, 15-20, 22-26 and 28-44 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Mitani, U.S. 6,633,956.

As presently written, the claims are quite broad, to the extent that they would have been taught by a system that utilized a random access memory to store logical-to-physical address mapping information for an associated flash memory, with all of the usual procedures utilized with such a map, such as reestablishing the map when a modification or erasure has occurred.

Mitani taught such a system. Note Figure 1.

(a) As for a "list" of addresses from which a free one may be selected, note the "management table" stored in RAM 4.

(b) As for the addresses representing "sectors", since flash memories are not radial disks, the term "sectors" is merely a convention to describe a given amount of data. In any case, the use of a sector as the amount of data in the flash memory is explicitly taught in column 3, lines 63 et seq.

(c) As for the selection of an address being "based on the ability of the physical sector to store the data without first being erased", selection of a free space (i.e., "available memory") instead of a full space clearly anticipates selecting "based on the ability of the physical sector to store the data without first being erased". Note column 9, lines 4 et seq.

(d) As for the claimed "forming" and "storing", this is simply entering the logical/physical address relationship into the table, as clearly taught throughout the reference.

(e) As for recreating the list or table after it has been erased (note Mitani, "After the status checks on the flash memories are complete, the physical addresses stored in the corresponding task registers are erased" – these task registers are in the RAM that stores the management table), this simply means re-entering the logical/physical address relationship into the table, which must be done by Mitani every time a relationship changes.

6. Claims 1-6, 15-20, 22-26 and 28-44 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Fujimoto et al., U.S. 6,377,500.

As presently written, the claims are quite broad, to the extent that they would have been taught by a system that utilized a random access memory to store logical-to-physical address mapping information for an associated flash memory, with all of the usual procedures utilized with such a map, such as reestablishing the map when a modification or erasure has occurred.

Fujimoto et al. taught such a system. Note Figures 1, 3 and 4A.

(a) As for a "list" of addresses from which a free one may be selected, note the LTPs in RAM 14.

(b) As for the addresses representing "sectors", since flash memories are not radial disks, the term "sectors" is merely a convention to describe a given amount of data. In any case, the use of sectors is mentioned *throughout* the reference. Note, e.g., column 1, lines 49 et seq. which gives an example of a 512 byte sector.

(c) As for the selection of an address being "based on the ability of the physical sector to store the data without first being erased", selection of a free space instead of a full space clearly anticipates selecting "based on the ability of the physical sector to store the data without first being erased". Note step S19 of Figure 6B.

(d) As for the claimed "forming" and "storing", this is simply entering the logical/physical address relationship into the table, as clearly taught throughout the reference.

(e) As for recreating the list or table after it has been erased, this simply means re-entering the logical/physical address relationship into the table, which must be done by Fujimoto et al. every time a relationship changes – this is clearly taught by the language "At least one of the tables is stored on a RAM ... a microprocessor determines whether a table corresponding to the logical address exists on the RAM. If such a table does not exist, the table is copies from the flash memory to the RAM).

Response to Amendment

7. With regard to the remarks attached to the amendment filed on May 21, 2004, these have been carefully considered by the examiner but are not deemed convincing. In the initial arguments, applicant's focus is on the breadth of the rejection and the detail to which the claim features are shown. However, the examiner wishes to note that the claims were, and still are, extremely broad. The claims represent a system of mapping that was not merely well known, but was *fundamental* to computer systems at the time of the invention.

The examiner is puzzled by such comments as "Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches or suggests the concept of a list of free physical sector addresses". How can this be possible when the feature is explicitly taught by the tables described in each reference? As described above, since flash memories are not radial disks, the term "sectors" is merely a convention to describe a given amount of data. Bruce et al., U.S. 6,000,006 even explains this in the Summary of the Invention "A 64 Mbit flash chip typically has 512-byte pages which happens to match the sector size for IDE and SCSI hard disks". The convention is similar to the use of "blocks" and "pages" in the art – each of these is a convention whose size is determined by the designer of a particular chip or system.

Applicant's have used similar language with regard to other features of the invention, but, for at least the reasons shown in the rejections above, the examiner is similarly puzzled as to how applicant was unable to locate these features, especially

since most of them were even described in the Summary of the Invention sections or even the Abstracts of the respective references. If the rejection seemed broad, it is because the claims had such a broad scope representing a fundamental technology. The examiner has elaborated the rejections in accordance with the features highlighted by applicant in the remarks attached to the amendment. Should any question arise regarding the rejection, applicant is invited to contact the examiner directly at the number provided below.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (703) 305-3824. The examiner is generally available between 8:00 am and 9:30 pm, EST, Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached at (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 746-7239 (Official communications)

or:

(703) 746-7240 (for Informal or Draft communications)

or:

(703) 746-7238 (for After-Final communications)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

B. James Peikari
Primary Examiner
Art Unit 2186

7/12/04